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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/799,201

03/12/2004

Jeoung-Mo Koo

8021-205 (SS-17942-US)

7424

22150 7590 03/09/2007
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EXAMINER

DIAZ, JOSE R

ART UNIT

PAPER NUMBER

2815

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

03/09/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,201	KOO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,6-8,16 and 24-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16 and 24-26 is/are allowed.
- 6) ☒ Claim(s) 1,2 and 6-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Wu et al. (US 5,633,520).

Regarding claim 1, Wu et al. teaches a one-time programmable memory device, comprising:

an isolation layer (FOX, 13, 13', 13'') for defining an active area of a substrate (10) [see figs. 1G and 5B];

an oxide layer (12, 12') formed on the active area [see figs. 1G and 5B];

a floating gate (FG, 14) formed over the active area and the isolation layer (13') [see figs. 1G and 5B];

an inter-gate dielectric layer (16) formed on the floating gate [see figs. 1G and 5B]; and

a control gate (C1, C2...Cn-1, Cn) formed on the inter-gate dielectric layer [see figs. 1G and 5B], wherein a first portion of the floating gate (consider the portion of layer 14 provided over gate dielectric 12 or 12' as shown in figures 1G and 5B) formed over the active area is narrower than a second portion of the floating gate formed over the isolation layer (consider the portion of layer 14 provided over isolation structure 13' as

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shown in figures 1G and 5B), and wherein the control gate (C1, C2...Cn-1, Cn) is formed over the second portion of the floating gate and not over the first portion of the floating gate [see figs. 1g and 5B], and wherein a plurality of edges of the control gate are formed to be within corresponding edges of the floating gate such that an area of the isolation layer overlapped by the second portion is greater than an area of the isolation layer overlapped by the control gate [consider the area covered by at least one of the Control gates (C1, C2...Cn-1, Cn) as shown in figs 1G and 5B].

Regarding claim 2, Wu et al. teaches a source region and a drain region (26, 28) formed in the active area at least one of under or adjacent both sides of the floating gate (N-MOS, P-MOS) [see fig. 2].

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 5,633,520) in view of Bhattacharya et al. (US Pat. No. 6,339,000 B1).

Regarding claim 6-8, Wu et al. fails to teach a three-layer inter-gate dielectric structure consisting of oxide, nitride and oxide. However, Bhattacharya et al. teaches that it is well known in the art to use a three-layer inter-gate dielectric structure consisting of oxide, nitride and oxide [col. 2, lines 14-20].

Wu et al. and Bhattacharya et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to include a three-layer inter-gate dielectric structure consisting of oxide, nitride and oxide. The motivation for doing so, as is taught by Bhattacharya et al., is to enhance the charge retention capability of the floating gate (col. 2, lines 11-20). Therefore, it would have been obvious to combine Bhattacharya et al. with Wu et al. to obtain the invention of claims 6-8.

Allowable Subject Matter

5. Claims 16 and 24-26 are allowed.
6. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a integrated circuit comprising a second gate oxide layer which is thinner than a tunnel oxide layer, and a first gate oxide layer which is thicker than the tunnel oxide layer and the second gate oxide layer as instantly claimed, and in combination with the additional limitations.

Response to Arguments

7. Applicant's arguments with respect to claims 1-2 and 6-8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fontana (US 4,823,173) discloses three areas on which a memory device and two transistors are formed over an oxide layer having multiple thicknesses (see abstract). Maserjian et al. (US 3,906,296) teaches control gates within edges of the floating gate (see abstract). Baumann (US 5,866,445) teaches two different gate oxide thicknesses for the PMOS and NMOS transistor [see col. 2 and lines 14-32].

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

José R. Díaz
Examiner
Art Unit 2815



KENNETH PARKER
SUPERVISORY PATENT EXAMINER